1. A non-volatile bit addressable memory array comprising a plurality of memory cells, each cell having:

a first control circuit having a transistor and receiving a bit line signal and word line signal, the first control circuit communicates with a select node based on the bit line signal and word line signal;

a second control circuit having a transistor and receiving the bit line signal and a release line signal, the second control circuit communicates with a restore node based on the bit line signal and a release line signal; and

an electromechanically deflectable three terminal switch comprising:

a first terminal connected to the select node;

a second terminal connected to the restore node; and

a third terminal connected to a reference signal and a deflectable nanotube article,

the nanotube article being electromechanically deflectable to contact the select node when a predetermined voltage difference is applied between the first and third terminals and being releasable from such contact when a predetermined voltage difference is applied between the second and third terminals.

2. The memory array according to claim 1, wherein the nanotube article is a ribbon of nanotube fabric.

3. The memory array according to claim 2 wherein each ribbon of nanotube fabric includes a plurality of carbon nanotubes.

4. The memory array of claim 2 wherein the nanotube fabric is porous.

5. The memory array of claim 2 wherein the nanotube fabric is substantially a monolayer of carbon nanotubes.

6. The memory array of claim 4 wherein the nanotube fabric is formed of single-walled carbon nanotubes.

7. The memory array of claim 1 wherein informational state of a memory cell is manifested by the position of the deflectable nanotube article and wherein the position of the nanotube switching element is sensed on the bit line as a time variation of the bit line signal.

8. The memory array of claim1 wherein the first control circuit is a FET receiving the bit line signal on a drain node and the word line signal on the gate node, and wherein the source is in electrical communication with the first terminal of the three terminal switch.

9. The memory array of claim1 wherein the second control circuit is a FET receiving the bit line signal on a drain node and the release line signal on the gate node, and wherein the source is in electrical communication with the second terminal of the three terminal switch.

10. The memory array of claim 1 wherein adjacent memory cells are arranged such that the second control circuit of one cell and the first control circuit of the other cell share a bit line

connection.

11. The memory array of claim 1 wherein the first control circuit is a first FET receiving the bit line signal on a drain node and the word line signal on the gate node, and wherein the source is in electrical communication with the first terminal of the three terminal switch, and wherein the second control circuit is a second FET receiving the bit line signal on a drain node and the release line signal on the gate node, and wherein the source is in electrical communication with the second terminal of the three terminal switch, and wherein adjacent memory cells are arranged such that the bit line connection is shared between the first and second FETs of adjacent cells.